

FIG. L

Reference Clock CLK2 CLK2 CLK3 CLK3 40 CLK3

To Clock distribution Network on Programmable Logic Device

Output Clocks with Dynamically reconfigurable frequencies

Configuration Controls

FIG. 2

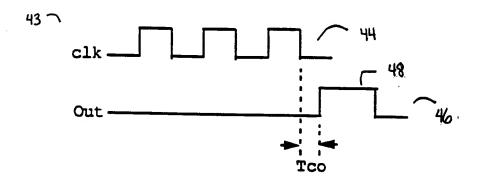
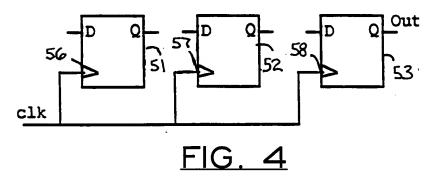


FIG. 3

(Falling Edge Triggered FFs)



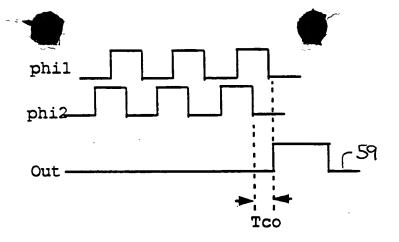


FIG. 5

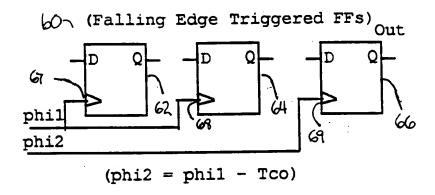


FIG. 6

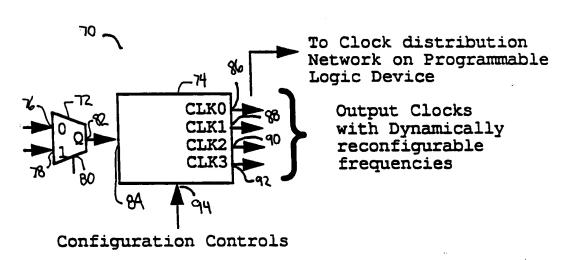


FIG. 7